**Cell Description:**This is a standard 4 input AND OR INVERT (AOI) cell. This cells functionality is described by the following Boolean equation:

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **Y** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "AOI22x1" "behavioral"

module AOI22X1( Y, A, B, C, D );

input A;

input B;

output Y;

input C;

input D;

assign Y = ~((A&B) | (C&D));

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

(C => Y) = (1.0, 1.0);

(D => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| AOI22X1 | 27.0 | 12.0 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI22X1 | 0.257172 | 3.554636 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI22X1 | 0.21.544 | 2.844555 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI22X1 | 0.280125 | 3.91496 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| AOI22X1 | 0.209476 | 3.092532 |

**Logic Symbol:**

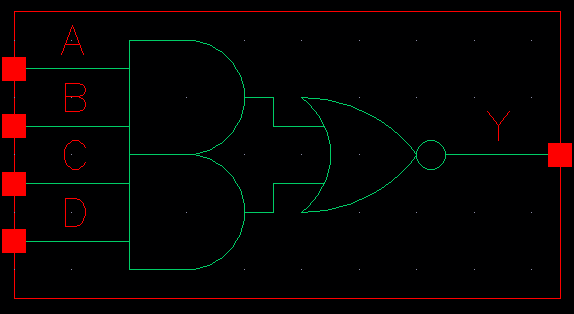
****

Figure : Symbol View for the AOI22 cell.

**CMOS Schematic:**

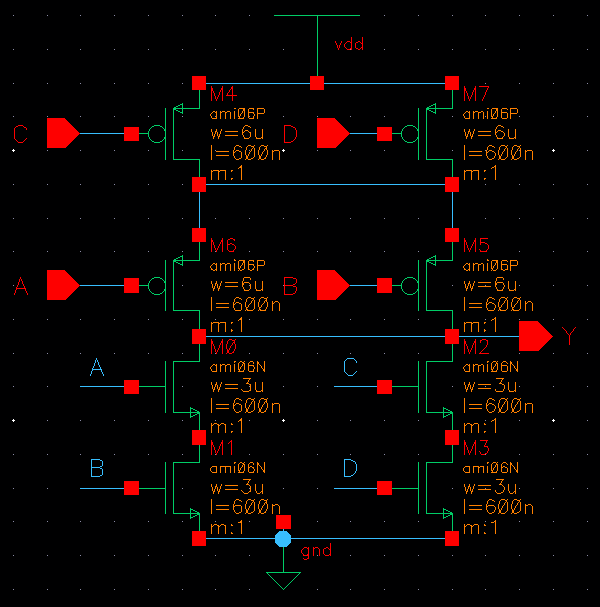
****

Figure : CMOS Schematic for the AOI22X1 cell.

**CMOS Layout:**

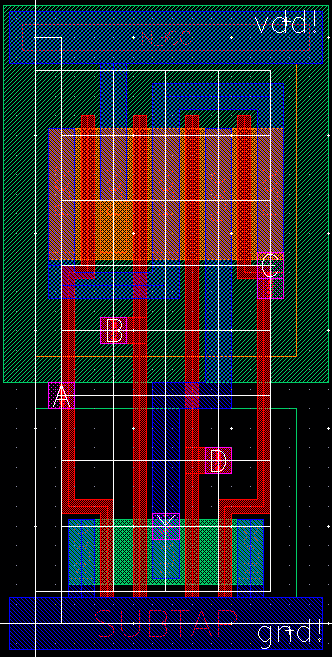
****

Figure : CMOS layout for the AOI22X1 cell.